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EXAMINER

CLEARY, THOMAS J

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 11/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/994,516

Applicant(s)

DOAN ET AL.

Examiner

Thomas J. Cleary

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-50 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-50 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 November 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>20040601; 20040820</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 2, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15, 16, 17, 19, 20, 21, 22, 23, 25, 26, 27, 28, 29, 30, 31, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over PCI System Architecture, Third Edition, by Tom Shanley ("Shanley"), US Patent Number 6,098,158 to Lay et al. ("Lay"), and Intel Application Note AP-758 'Flash Memory PCI Add-In Card for Embedded Systems' ("AP-758").

3. In reference to Claim 1, Shanley teaches a central processing unit (CPU) (See Figure 2-3 'CPU'); a first bus coupled to the CPU (See Figure 2-3 'CPU Local Bus'); a memory coupled to the first bus to store data accessible by the CPU via the first bus (See Figure 2-3 'Main Memory'); a second bus coupled to the first bus to provide communication with the CPU and the memory via the first bus (See Figure 2-3 'PCI Bus'); and a PC card coupled to the second bus (See Figure 2-3). Shanley does not

teach the PC card having a non-volatile memory for storing machine state information and further having a controller coupled to the non-volatile memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system. AP-758 teaches a PC card having a non-volatile memory (See Page 1 Section 1.0). Lay teaches storing machine state information in a non-volatile memory (See Figure 4 and Column 2 Line 23 – Column 3 Line 5) and a controller coupled to the non-volatile memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Column 2 Lines 26-31, Column 2 Lines 45-54, and Column 3 Lines 2-5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 1, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

4. In reference to Claim 2, Shanley, AP-758, and Lay teach the limitations as applied to Claim 1 above. Shanley further teaches that the first bus comprises a local CPU bus (See Figure 2-3 'CPU Local Bus') and the second bus comprises a PCI bus (See Figure 2-3 'PCI Bus').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 2, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

5. In reference to Claim 4, Shanley, AP-758, and Lay teach the limitations as applied to Claim 1 above. AP-758 further teaches that the non-volatile memory of the PC card comprises a flash memory device (See Page 1 Section 1.0 Paragraphs 2-7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system

state to non-volatile memory of Lay, resulting in the invention of Claim 4, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

6. In reference to Claim 5, Shanley, AP-758, and Lay teach the limitations as applied to Claim 1 above. AP-758 further teaches that the PC card further includes a bus interface coupled to the second bus, and further coupled to the non-volatile memory and the controller to transfer data between the non-volatile memory and the second bus in accordance with a data format and transfer protocol of the second bus. (See Page 2 Figure 2 and Page 3 Paragraph 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 5, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See

Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

7. In reference to Claim 6, Shanley, AP-758, and Lay teach the limitations as applied to Claim 1 above. Lay further teaches a transfer component directing the controller to coordinate access between the non-volatile memory and the memory to transfer machine state information (See Figures 4 and 6, Column 2 Lines 26-31, Column 2 Lines 45-54, Column 3 Lines 2-5, and Column 5 Lines 39-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 6, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

8. In reference to Claim 7, Shanley, AP-758, and Lay teach the limitations as applied to Claim 1 above. Shanley, AP-758, and Lay do not teach compression and decompression components for compressing the machine state information to be stored

and decompressing the stored compressed machine state information to be downloaded, respectively. Lay, however, teaches that it is well known to compress an image of the machine state information to be saved to disk, and to later decompress the image when booting the system (See Column 1 Lines 51-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, and the compression and decompression of a boot image of Lay, resulting in the invention of Claim 7, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay), to decrease boot time (See Column 1 Lines 56-58), and because it is well known that compressed data takes up less space in memory than uncompressed data, thus allowing more efficient use of the memory space.

9. In reference to Claim 8, Shanley, AP-758, and Lay teach the limitations as applied to Claim 1 above. Lay further teaches that the machine state information comprises data from the memory and CPU for returning the computer system to the

same condition of operability as when the machine state information was stored in the non-volatile memory (See Figure 3 and Column 2 Lines 26-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 8, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

10. In reference to Claim 9, Shanley teaches a central processing unit (CPU) (See Figure 2-3 'CPU'); a memory coupled to the CPU to store data accessible by the CPU (See Figure 2-3 'Main Memory'); a bus coupled to the CPU and the memory to provide communication therewith (See Figure 2-3 'PCI Bus'); and a PC card coupled to the bus (See Figure 2-3). Shanley does not teach the PC card having a non-volatile memory for storing machine state information and further having a controller coupled to the non-volatile memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system. AP-758

teaches a PC card having a non-volatile memory (See Page 1 Section 1.0). Lay teaches storing machine state information in a non-volatile memory (See Figure 4 and Column 2 Line 23 – Column 3 Line 5) and a controller coupled to the non-volatile memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Column 2 Lines 26-31, Column 2 Lines 45-54, and Column 3 Lines 2-5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 9, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

11. In reference to Claim 11, Shanley, AP-758, and Lay teach the limitations as applied to Claim 9 above. AP-758 further teaches that the non-volatile memory of the PC card comprises a flash memory device (See Page 1 Section 1.0 Paragraphs 2-7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 11, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

12. In reference to Claim 12, Shanley, AP-758, and Lay teach the limitations as applied to Claim 9 above. AP-758 further teaches that the PC card further includes a bus interface coupled to the bus, and further coupled to the non-volatile memory and the controller to transfer data between the non-volatile memory and the bus in accordance with a data format and transfer protocol of the bus. (See Page 2 Figure 2 and Page 3 Paragraph 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 12, in order to allow the system to function as an embedded system (See Page 1 Section 1.0

Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

13. In reference to Claim 13, Shanley, AP-758, and Lay teach the limitations as applied to Claim 9 above. Lay further teaches a transfer component directing the controller to coordinate access between the non-volatile memory and the memory to transfer machine state information (See Figures 4 and 6, Column 2 Lines 26-31, Column 2 Lines 45-54, Column 3 Lines 2-5, and Column 5 Lines 39-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 13, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

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14. In reference to Claim 14, Shanley, AP-758, and Lay teach the limitations as applied to Claim 9 above. Shanley, AP-758, and Lay do not teach compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively. Lay, however, teaches that it is well known to compress an image of the machine state information to be saved to disk, and to later decompress the image when booting the system (See Column 1 Lines 51-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, and the compression and decompression of a boot image of Lay, resulting in the invention of Claim 14, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay), to decrease boot time (See Column 1 Lines 56-58), and because it is well known that compressed data takes up less space in memory than uncompressed data, thus allowing more efficient use of the memory space.

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15. In reference to Claim 15, Shanley, AP-758, and Lay teach the limitations as applied to Claim 9 above. Lay further teaches that the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory (See Figure 3 and Column 2 Lines 26-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 15, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

16. In reference to Claim 16, Shanley teaches an apparatus having a central processing unit (CPU) (See Figure 2-3 'CPU') coupled to a memory (See Figure 2-3 'Main Memory') via a first bus (See Figure 2-3 'CPU Local Bus'), and further having a second bus coupled to the first bus to provide communication with the CPU and the memory (See Figure 2-3 'PCI Bus'); and a PC card coupled to the second bus (See Figure 2-3). Shanley does not teach that the apparatus is for capturing and restoring a

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machine state of a computer system, the PC card having a non-volatile memory for storing machine state information corresponding to the machine state, and further having a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom; and a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system. AP-758 teaches a PC card having a non-volatile memory (See Page 1 Section 1.0). Lay teaches storing machine state information in a non-volatile memory (See Figure 4 and Column 2 Line 23 – Column 3 Line 5); a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom (See Column 2 Lines 26-31, Column 2 Lines 45-54, and Column 3 Lines 2-5); and a transfer component directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Figures 4 and 6, Column 2 Lines 26-31, Column 2 Lines 45-54, Column 3 Lines 2-5, and Column 5 Lines 39-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 16, in order to allow the system to function as an embedded system (See Page 1 Section 1.0

Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

17. In reference to Claim 17, Shanley, AP-758, and Lay teach the limitations as applied to Claim 16 above. AP-758 further teaches that the PC card further includes a bus interface coupled to the second bus, and further coupled to the non-volatile memory and the controller to transfer data between the non-volatile memory and the second bus in accordance with a data format and transfer protocol of the second bus. (See Page 2 Figure 2 and Page 3 Paragraph 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 16, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758); because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

18. In reference to Claim 19, Shanley, AP-758, and Lay teach the limitations as applied to Claim 16 above. AP-758 further teaches that the non-volatile memory comprises a flash memory (See Page 1 Section 1.0 Paragraphs 2-7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 19, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

19. In reference to Claim 20, Shanley, AP-758, and Lay teach the limitations as applied to Claim 16 above. Lay further teaches the transfer component comprises: a storing component for directing the controller to store machine state information from the CPU and memory to the non-volatile memory (See Figure 3, Column 2 Lines 26-31, and Column 2 Lines 45-54); and a download component for directing the controller to transfer data from the nonvolatile memory to the CPU and the memory (See Figure 5, Column 3 Lines 2-5, and Column 5 Lines 32-63).

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It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 20, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

20. In reference to Claim 21, Shanley, AP-758, and Lay teach the limitations as applied to Claim 16 above. Shanley, AP-758, and Lay do not teach compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively. Lay, however, teaches that it is well known to compress an image of the machine state information to be saved to disk, and to later decompress the image when booting the system (See Column 1 Lines 51-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, and the compression and decompression of a boot

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image of Lay, resulting in the invention of Claim 21, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay), to decrease boot time (See Column 1 Lines 56-58), and because it is well known that compressed data takes up less space in memory than uncompressed data, thus allowing more efficient use of the memory space.

21. In reference to Claim 22, Shanley teaches an apparatus having a central processing unit (CPU) (See Figure 2-3 'CPU') coupled to a memory (See Figure 2-3 'Main Memory'), and further having a bus coupled to the CPU and memory to provide communication with the CPU and the memory (See Figure 2-3 'PCI Bus'); and a PC card coupled to the second bus (See Figure 2-3). Shanley does not teach that the apparatus is for capturing and restoring a machine state of a computer system, the PC card having a non-volatile memory for storing machine state information corresponding to the machine state, and further having a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom; and a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer

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system. AP-758 teaches a PC card having a non-volatile memory (See Page 1 Section 1.0). Lay teaches storing machine state information in a non-volatile memory (See Figure 4 and Column 2 Line 23 – Column 3 Line 5); a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom (See Column 2 Lines 26-31, Column 2 Lines 45-54, and Column 3 Lines 2-5); and a transfer component directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Figures 4 and 6, Column 2 Lines 26-31, Column 2 Lines 45-54, Column 3 Lines 2-5, and Column 5 Lines 39-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 22, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

22. In reference to Claim 23, Shanley, AP-758, and Lay teach the limitations as applied to Claim 22 above. AP-758 further teaches that the PC card further includes a bus interface coupled to the bus, and further coupled to the non-volatile memory and the controller to transfer data between the non-volatile memory and the bus in accordance with a data format and transfer protocol of the second bus. (See Page 2 Figure 2 and Page 3 Paragraph 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 23, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

23. In reference to Claim 25, Shanley, AP-758, and Lay teach the limitations as applied to Claim 23 above. AP-758 further teaches that the non-volatile memory comprises a flash memory (See Page 1 Section 1.0 Paragraphs 2-7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile

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flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 25, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

24. In reference to Claim 26, Shanley, AP-758, and Lay teach the limitations as applied to Claim 23 above. Lay further teaches the transfer component comprises: a storing component for directing the controller to store machine state information from the CPU and memory to the non-volatile memory (See Figure 3, Column 2 Lines 26-31, and Column 2 Lines 45-54); and a download component for directing the controller to transfer data from the nonvolatile memory to the CPU and the memory (See Figure 5, Column 3 Lines 2-5, and Column 5 Lines 32-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 26, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface

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that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

25. In reference to Claim 27, Shanley, AP-758, and Lay teach the limitations as applied to Claim 23 above. Shanley, AP-758, and Lay do not teach compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively. Lay, however, teaches that it is well known to compress an image of the machine state information to be saved to disk, and to later decompress the image when booting the system (See Column 1 Lines 51-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, and the compression and decompression of a boot image of Lay, resulting in the invention of Claim 27, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), to allow the system to boot up faster (See Column 1 Lines 39-

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50 and Column 2 Lines 23-40 of Lay), to decrease boot time (See Column 1 Lines 56-58), and because it is well known that compressed data takes up less space in memory than uncompressed data, thus allowing more efficient use of the memory space.

26. In reference to Claim 38, Shanley teaches a computer system having a central processing unit (CPU) (See Figure 2-3 'CPU') coupled to a memory (See Figure 2-3 'Main Memory'), and further having a bus coupled to the CPU and memory to provide communication therewith (See Figure 2-3 'PCI Bus'), and a PC card (See Figure 2-3). Shanley does not teach a method for storing a machine state of the computer system, comprising: capturing the machine state of the computer system; transferring machine state information corresponding to the captured machine state from the computer system to a PC card having a non-volatile memory; and storing the machine state information in the non-volatile memory in order to restore the stored machine state when the machine state information is provided to a computer system. AP-758 teaches a PC card having a non-volatile memory (See Page 1 Section 1.0). Lay teaches capturing the machine state of the computer system (See Column 2 Lines 26-37); transferring machine state information corresponding to the captured machine state from the computer system to a non-volatile memory (See Figure 4 and Column 2 Line 23 – Column 3 Line 5); and storing the machine state information in the non-volatile memory in order to restore the stored machine state when the machine state information is provided to a computer system (See Figure 4 and Column 2 Line 23 – Column 3 Line 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 38, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

27. In reference to Claim 39, Shanley, AP-758, and Lay teach the limitations as applied to Claim 38 above. Lay further teaches that capturing, transferring and storing the machine state information is in response to executing a power down procedure (See Column 4 Lines 20-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 39, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good

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performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

28. In reference to Claim 40, Shanley, AP-758, and Lay teach the limitations as applied to Claim 38 above. Lay further teaches that capturing, transferring and storing the machine state information is in response to a user request (See Column 4 Lines 20-25, Column 4 Lines 41-55, and Column 5 Lines 36-38).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 40, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

29. In reference to Claim 41, Shanley, AP-758, and Lay teach the limitations as applied to Claim 38 above. Lay further teaches that the machine state information comprises data from the memory and CPU for returning the computer system to the

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same condition of operability as when the machine state information was stored in the non-volatile memory (See Figure 3 and Column 2 Lines 26-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 41, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

30. In reference to Claim 42, Shanley, AP-758, and Lay teach the limitations as applied to Claim 38 above. Lay further teaches that capturing the machine state of the computer system comprises: capturing data present in the memory (See Column 2 Lines 33-37); and capturing data present in registers of the CPU (See Column 5 Lines 1-6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 42, in order to

allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

31. In reference to Claim 44, Shanley, AP-758, and Lay teach the limitations as applied to Claim 38 above. Shanley, AP-758, and Lay do not teach compressing the machine state information to be stored in the non-volatile memory. Lay, however, teaches that it is well known to compress an image of the machine state information to be saved to disk, and to later decompress the image when booting the system (See Column 1 Lines 51-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, and the compression and decompression of a boot image of Lay, resulting in the invention of Claim 44, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0

Paragraph 5 of AP-758), to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay), to decrease boot time (See Column 1 Lines 56-58), and because it is well known that compressed data takes up less space in memory than uncompressed data, thus allowing more efficient use of the memory space.

32. In reference to Claim 45, Shanley teaches a computer system having a central processing unit (CPU) (See Figure 2-3 'CPU') coupled to a memory (See Figure 2-3 'Main Memory'), and further having a bus coupled to the CPU and memory to provide communication therewith (See Figure 2-3 'PCI Bus'), and a PC card (See Figure 2-3). Shanley does not teach a method for restoring a machine state of the computer system, comprising: identifying machine state information corresponding to the machine state to which the computer system is to be restored stored in a non-volatile memory included in a PC card; transferring the machine state information from the non-volatile memory to the computer system; and writing data of the machine state information to the memory and CPU in order to restore the computer system to the identified machine state. AP-758 teaches a PC card having a non-volatile memory (See Page 1 Section 1.0). Lay teaches identifying machine state information corresponding to the machine state to which the computer system is to be restored stored in a non-volatile memory (See Column 5 Lines 41-44) ; transferring the machine state information from the non-volatile memory to the computer system (See Figure 6 and Column 5 Lines 44-46); and writing data of the machine state information to the memory and CPU in order to restore the

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computer system to the identified machine state (See Figures 5 and 6 and Column 5 Lines 53-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 45, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

33. In reference to Claim 46, Shanley, AP-758, and Lay teach the limitations as applied to Claim 45 above. Lay further teaches that identifying, transferring and writing the machine state information is in response to executing a power up procedure (See Column 4 Lines 20-25 and Column 5 Lines 32-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 46, in order to allow the system to function as an embedded system (See Page 1 Section 1.0

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Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

34. In reference to Claim 47, Shanley, AP-758, and Lay teach the limitations as applied to Claim 45 above. Lay further teaches that identifying, transferring and writing the machine state information is in response to a user request (See Column 4 Lines 20-25, Column 4 Lines 41-55, and Column 5 Lines 36-38).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 47, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

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35. In reference to Claim 48, Shanley, AP-758, and Lay teach the limitations as applied to Claim 45 above. Lay further teaches that the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory (See Figure 3 and Column 2 Lines 26-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, resulting in the invention of Claim 41, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), and to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay).

36. In reference to Claim 50, Shanley, AP-758, and Lay teach the limitations as applied to Claim 45 above. Shanley, AP-758, and Lay do not teach that the machine state information stored in the non-volatile memory is in a compressed data format, and the method further comprises decompressing the machine state information to be transferred to the computer system. Lay, however, teaches that it is well known to

compress an image of the machine state information to be saved to disk, and to later decompress the image when booting the system (See Column 1 Lines 51-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758 and the fast boot by saving the system state to non-volatile memory of Lay, and the compression and decompression of a boot image of Lay, resulting in the invention of Claim 50, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay), to decrease boot time (See Column 1 Lines 56-58), and because it is well known that compressed data takes up less space in memory than uncompressed data, thus allowing more efficient use of the memory space.

37. Claims 3, 10, 18, 24, 43, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shanley, AP-758, and Lay as applied to Claims 2, 9, 17, 23, 39, and 46 above, and further in view of US Patent Number 6,256,692 Yoda et al. ("Yoda").

38. In reference to Claim 3, Shanley, AP-758, and Lay teach the limitations as applied to Claim 1 above. Shanley, AP-758, and Lay do not teach a PCI-CardBus

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bridge coupled to the PCI bus to provide communication between the PCI bus and a CardBus compatible device coupled to the PCI-CardBus bridge. AP-758 teaches placing non-volatile memory on a removable PCI card (See Page 1 Section 1.0). Yoda teaches connecting a non-volatile memory device to a CardBus (See Column 4 Lines 64-66) and connecting the CardBus through a bridge to a PCI bus (See Figure 2 Number 24, Column 1 Lines 7-12, Column 2 Lines 13-30, and Column 4 Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Shanley, AP-758, and Lay with the CardBus device connected to a PCI bus of Yoda, resulting in the invention of Claim 3, because CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

39. In reference to Claim 10, Shanley, AP-758, and Lay teach the limitations as applied to Claim 9 above. Shanley further teaches that the bus comprises a PCI bus (See Figure 2-3 'PCI Bus'). Shanley, AP-758, and Lay do not teach that the computer system further comprises a PCI-CardBus bridge coupled to the PCI bus to provide communication between the PCI bus and a CardBus compatible device coupled to the PCI-CardBus bridge. AP-758 teaches placing non-volatile memory on a removable PCI card (See Page 1 Section 1.0). Yoda teaches connecting a non-volatile memory device to a CardBus (See Column 4 Lines 64-66) and connecting the CardBus through

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a bridge to a PCI bus (See Figure 2 Number 24, Column 1 Lines 7-12, Column 2 Lines 13-30, and Column 4 Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Shanley, AP-758, and Lay with the CardBus device connected to a PCI bus of Yoda, resulting in the invention of Claim 10, because CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

40. In reference to Claim 18, Shanley, AP-758, and Lay teach the limitations as applied to Claim 17 above. Shanley further teaches that the second bus is a PCI bus (See Figure 2-3 'PCI Bus'). Shanley, AP-758, and Lay do not teach that the bus interface is CardBus compatible. AP-758 teaches placing non-volatile memory on a removable PCI card (See Page 1 Section 1.0). Yoda teaches connecting a non-volatile memory device to a CardBus (See Column 4 Lines 64-66) and connecting the CardBus through a bridge to a PCI bus (See Figure 2 Number 24, Column 1 Lines 7-12, Column 2 Lines 13-30, and Column 4 Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Shanley, AP-758, and Lay with the CardBus device connected to a PCI bus of Yoda, resulting in the invention of Claim 18, because CardBus devices provide the same facilities as PCI devices and allows the

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devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

41. In reference to Claim 24, Shanley, AP-758, and Lay teach the limitations as applied to Claim 23 above. Shanley further teaches that the bus is a PCI bus (See Figure 2-3 'PCI Bus'). Shanley, AP-758, and Lay do not teach that the bus interface is CardBus compatible. AP-758 teaches placing non-volatile memory on a removable PCI card (See Page 1 Section 1.0). Yoda teaches connecting a non-volatile memory device to a CardBus (See Column 4 Lines 64-66) and connecting the CardBus through a bridge to a PCI bus (See Figure 2 Number 24, Column 1 Lines 7-12, Column 2 Lines 13-30, and Column 4 Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Shanley, AP-758, and Lay with the CardBus device connected to a PCI bus of Yoda, resulting in the invention of Claim 24, because CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

42. In reference to Claim 43, Shanley, AP-758, and Lay teach the limitations as applied to Claim 38 above. Shanley, AP-758, and Lay do not teach that transferring the machine state information to the PC card comprises transferring data from the CPU and the memory to the PC card in accordance with a CardBus protocol. AP-758 teaches

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placing non-volatile memory on a removable PCI card (See Page 1 Section 1.0). Yoda teaches connecting a non-volatile memory device to a CardBus (See Column 4 Lines 64-66) and connecting the CardBus through a bridge to a PCI bus (See Figure 2 Number 24, Column 1 Lines 7-12, Column 2 Lines 13-30, and Column 4 Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Shanley, AP-758, and Lay with the CardBus device connected to a PCI bus of Yoda, resulting in the invention of Claim 43, because CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

43. In reference to Claim 49, Shanley, AP-758, and Lay teach the limitations as applied to Claim 45 above. Shanley, AP-758, and Lay do not teach that transferring the machine state information from the non-volatile memory comprises transferring data from the PC card to the computer system in accordance with a CardBus protocol. AP-758 teaches placing non-volatile memory on a removable PCI card (See Page 1 Section 1.0). Yoda teaches connecting a non-volatile memory device to a CardBus (See Column 4 Lines 64-66) and connecting the CardBus through a bridge to a PCI bus (See Figure 2 Number 24, Column 1 Lines 7-12, Column 2 Lines 13-30, and Column 4 Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Shanley, AP-758, and Lay with the

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CardBus device connected to a PCI bus of Yoda, resulting in the invention of Claim 49, because CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

44. Claims 28, 29, 30, 31, 32, 33, 34, 35, 36, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shanley, Lay, AP-758, and Yoda.

45. In reference to Claim 28, Shanley teaches a computer system having a central processing unit (CPU) (See Figure 2-3 'CPU') coupled to a memory (See Figure 2-3 'Main Memory') via a CPU bus (See Figure 2-3 'CPU Local Bus'), and further having a PCI bus coupled to the CPU bus to provide communication with the CPU and the memory (See Figure 2-3 'PCI Bus'); and a PC card comprising an interface coupled to the PCI bus for transferring data thereto and therefrom (See Figure 2-3). Shanley does not teach that the PC card is a CardBus compatible PC card for restoring a machine state of a computer system, the PC card having a non-volatile memory coupled to the interface for storing and providing machine state information corresponding to the machine state; a controller coupled to the interface and non-volatile memory to control the storing of machine state data in the non-volatile memory and the retrieval of machine state information from the non-volatile memory; and a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory

and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system. AP-758 teaches a PC card having a non-volatile memory (See Page 1 Section 1.0). Lay teaches storing machine state information in a non-volatile memory (See Figure 4 and Column 2 Line 23 – Column 3 Line 5) and a controller coupled to the non-volatile memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Column 2 Lines 26-31, Column 2 Lines 45-54, and Column 3 Lines 2-5); and a transfer component directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Figures 4 and 6, Column 2 Lines 26-31, Column 2 Lines 45-54, Column 3 Lines 2-5, and Column 5 Lines 39-63). Yoda teaches connecting a non-volatile memory device to a CardBus (See Column 4 Lines 64-66) and connecting the CardBus through a bridge to a PCI bus (See Figure 2 Number 24, Column 1 Lines 7-12, Column 2 Lines 13-30, and Column 4 Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758, the fast boot by saving the system state to non-volatile memory of Lay, and the CardBus device connected to a PCI bus of Yoda, resulting in the invention of Claim 28, in order to allow the system to function as

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an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay), and because CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

46. In reference to Claim 29, Shanley, AP-758, Lay, and Yoda teach the limitations as applied to Claim 28 above. Lay further teaches that the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory (See Figure 3 and Column 2 Lines 26-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758, the fast boot by saving the system state to non-volatile memory of Lay, and the CardBus device connected to a PCI bus of Yoda, resulting in the invention of Claim 29, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset

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technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay), and because CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

47. In reference to Claim 30, Shanley, AP-758, Lay, and Yoda teach the limitations as applied to Claim 1 above. AP-758 further teaches that the non-volatile memory of the PC card comprises a flash memory device (See Page 1 Section 1.0 Paragraphs 2-7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758, the fast boot by saving the system state to non-volatile memory of Lay, and the CardBus device connected to a PCI bus of Yoda, resulting in the invention of Claim 30, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), to allow the system to boot up faster (See Column 1 Lines 39-50 and

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Column 2 Lines 23-40 of Lay), and because CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

48. In reference to Claim 31, Shanley, AP-758, Lay, and Yoda teach the limitations as applied to Claim 28 above. Lay further teaches the transfer component comprises: a storing component for directing the controller to store machine state information from the CPU and memory to the non-volatile memory (See Figure 3, Column 2 Lines 26-31, and Column 2 Lines 45-54); and a download component for directing the controller to transfer data from the nonvolatile memory to the CPU and the memory (See Figure 5, Column 3 Lines 2-5, and Column 5 Lines 32-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758, the fast boot by saving the system state to non-volatile memory of Lay, and the CardBus device connected to a PCI bus of Yoda, resulting in the invention of Claim 31, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), to allow the system to boot up faster (See Column 1 Lines 39-50 and

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Column 2 Lines 23-40 of Lay), and because CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

49. In reference to Claim 32, Shanley, AP-758, Lay, and Yoda teach the limitations as applied to Claim 28 above. Shanley, AP-758, Lay, and Yoda do not teach compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively. Lay, however, teaches that it is well known to compress an image of the machine state information to be saved to disk, and to later decompress the image when booting the system (See Column 1 Lines 51-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758, the fast boot by saving the system state to non-volatile memory of Lay, the compression and decompression of a boot image of Lay, and the CardBus device connected to a PCI bus of Yoda, resulting in the invention of Claim 32, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), to allow the system to boot up

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faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay), to decrease boot time (See Column 1 Lines 56-58), because it is well known that compressed data takes up less space in memory than uncompressed data, thus allowing more efficient use of the memory space, and because CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

50. In reference to Claim 33, Shanley teaches a computer system comprising a central processing unit (CPU) (See Figure 2-3 'CPU'); a local CPU bus coupled to the CPU (See Figure 2-3 'CPU Local Bus'); a memory coupled to the local CPU bus to store data accessible by the CPU via the local CPU bus (See Figure 2-3 'Main Memory'); a PCI bus coupled to the local CPU bus to provide communication with the CPU and the memory via the local CPU bus (See Figure 2-3 'PCI Bus'); and a PC card (See Figure 2-3). Shanley does not teach a PCI-CardBus bridge coupled to the PCI bus to provide communication between the PCI bus and a CardBus compatible device; a CardBus compatible PC card coupled to PCI-CardBus bridge, the PC card having a non-volatile memory for storing machine state information corresponding to the machine state, and further having a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom; and a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and

restoring, respectively, a corresponding machine state of a computer system. AP-758 teaches a PC card having a non-volatile memory (See Page 1 Section 1.0). Lay teaches storing machine state information in a non-volatile memory (See Figure 4 and Column 2 Line 23 – Column 3 Line 5); controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom (See Column 2 Lines 26-31, Column 2 Lines 45-54, and Column 3 Lines 2-5); and a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Figures 4 and 6, Column 2 Lines 26-31, Column 2 Lines 45-54, Column 3 Lines 2-5, and Column 5 Lines 39-63). Yoda teaches connecting a non-volatile memory device to a CardBus (See Column 4 Lines 64-66) and connecting the CardBus through a bridge to a PCI bus (See Figure 2 Number 24, Column 1 Lines 7-12, Column 2 Lines 13-30, and Column 4 Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758, the fast boot by saving the system state to non-volatile memory of Lay, and the CardBus device connected to a PCI bus of Yoda, resulting in the invention of Claim 33, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard

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protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay), and because CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

51. In reference to Claim 34, Shanley, AP-758, Lay, and Yoda teach the limitations as applied to Claim 33 above. AP-758 further teaches that the non-volatile memory of the PC card comprises a flash memory device (See Page 1 Section 1.0 Paragraphs 2-7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758, the fast boot by saving the system state to non-volatile memory of Lay, and the CardBus device connected to a PCI bus of Yoda, resulting in the invention of Claim 34, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay), and because CardBus devices provide the same

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facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

52. In reference to Claim 35, Shanley, AP-758, Lay, and Yoda teach the limitations as applied to Claim 33 above. AP-758 further teaches that the PC card further includes a bus interface coupled to the PCI bus, and further coupled to the non-volatile memory and the controller to transfer data between the memory and the PCI bus in accordance with the PCI data format and transfer protocol (See Pages 1-2 and Figures 1-2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758, the fast boot by saving the system state to non-volatile memory of Lay, and the CardBus device connected to a PCI bus of Yoda, resulting in the invention of Claim 35, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay), and because CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business

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card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

53. In reference to Claim 36, Shanley, AP-758, Lay, and Yoda teach the limitations as applied to Claim 33 above. Shanley, AP-758, Lay, and Yoda do not teach compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively. Lay, however, teaches that it is well known to compress an image of the machine state information to be saved to disk, and to later decompress the image when booting the system (See Column 1 Lines 51-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758, the fast boot by saving the system state to non-volatile memory of Lay, the compression and decompression of a boot image of Lay, and the CardBus device connected to a PCI bus of Yoda, resulting in the invention of Claim 36, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay), to decrease boot time (See Column 1 Lines 56-58), because it is well known that compressed data takes

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up less space in memory than uncompressed data, thus allowing more efficient use of the memory space, and because CardBus devices provide the same facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

54. In reference to Claim 37, Shanley, AP-758, Lay, and Yoda teach the limitations as applied to Claim 33 above. Lay further teaches that the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory (See Figure 3 and Column 2 Lines 26-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Shanley with the non-volatile flash memory located on a PC card of AP-758, the fast boot by saving the system state to non-volatile memory of Lay, and the CardBus device connected to a PCI bus of Yoda, resulting in the invention of Claim 37, in order to allow the system to function as an embedded system (See Page 1 Section 1.0 Paragraph 1 of AP-758), because the PCI bus presents an easy to implement interface that can use current chipset technologies from the host processor bus, has good performance, industry standard protocols, and provisions for system boot control (See Page 1 Section 1.0 Paragraph 5 of AP-758), to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay), and because CardBus devices provide the same

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facilities as PCI devices and allows the devices to be configured as a card of a business card size rather than for fitting onto a printed substrate as with PCI devices (See Column 1 Lines 32-38 of Yoda).

Information Disclosure Statement

55. Applicant's assistance is requested in identifying any prior art believed to be of particular relevance to the current application.

Response to Amendment

56. The declaration filed on 3 September 2004 under 37 CFR 1.131 is sufficient to overcome the Coulson reference.

Conclusion

57. The following prior art made of record and not relied upon is considered pertinent to Applicant's disclosure: US Patent Number 4,930,128 to Suzuki et al.; US Patent Number 5,269,022 to Shinjo et al.; US Patent Number 5,317,752 to Jewett et al.; US Patent Number 5,577,220 to Combs et al.; US Patent Number 5,715,456 to Bennett et al.; US Patent Number 6,256,692 to Yoda et al; US Patent Number 6,434,696 to Kang; US Patent Number 6,807,630 to Lay et al.; US Patent Application Publication Number

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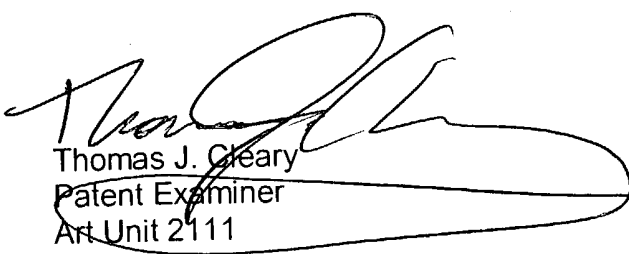
2001/0039612 to Lee; and US Patent Application Publication Number 2002/0116588 to Beckert et al.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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